ABSTRACT

Test logic supports the testing of an electronic circuit, where the number of ports of the electronic circuit exceeds the number of available tester IO channels. In some examples, the test logic utilizes observe logic in order to analyze the output ports that are masked so that the number of tester IO channels need not be expanded. Digital data from an electronic circuit is compacted by processing the data with a signature compactor to determine a signature corresponding to the output data. A comparator may compare the determined signature with the correct signature to provide a "go/no-go" indication to a process through a processor channel. Providing test coverage using a signature averts the necessity of having additional tester IO channels to cover the associated section of the electronic circuit. Additionally, a pattern generator may be supported by the test logic to provide digital activity for the electronic circuit.